20.1 3D Capacitive Interconnections with Mono- and Bi-Directional Capabilities

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3D integration is a key technology for the implementation of complex systems; heterogeneous process integration, simplified routing, volume and footprint reduction are some of the features that take advantage of stacking and vertically connecting dies. This work focuses on contactless interconnections based on capacitive coupling. Fig. 20.1.1 sketches the principle of 3D capacitive connectivity and presents photos with examples of the assembly approach used. Dies are stacked face-to-face leaving the standard I/O pads uncovered; electrodes in the upper metal layer provide coupling between TX-RX circuits. For mechanical stability and inter-chip isolation, a 1μm layer of acrylate-based adhesive is sandwiched between the dies. Previously, [1] demonstrated a bandwidth of 900Mb/s/pin with an interconnection area down to 8×8μm^2 and an energy consumption of 0.14mW/Gb/s. This work presents an asynchronous communication scheme, with significantly improved mono- and bi-directional transmission capabilities.

Circuits for asynchronous interconnections are sketched in Fig. 20.1.2. The transmitter is a buffer that drives the electrode. The receiver implements a double feed-back topology that provides voltage recovery as well as high-impedance for the AC input. The inverter N4-P4 amplifies the input signal and generates the *Recovery Enable* signal. This determines a positive feedback on the electrode (transistors N3, P3) that recovers the correct voltage level for the related logic state. After an appropriate delay, the received signal reaches $\overline{Z}$ and the feed-back is switched off (N2, P2) leaving the electrode in a high impedance state. The diode connected transistors P1 and N1 reduce the voltage swing of the electrode and keep it close to the logic threshold of the amplification stage (N4-P4) while limiting the direct leakage current. P1 and N1 are low-V_T (V_{TL}) transistors while N4 and P4 are high-V_T (V_{TH}) devices, so the leakage of N4 and P4 is reduced thanks to a positive cut-off (V_{TH}-V_{TL}). The mix of devices with different threshold prevents wrong commutations, even at low frequency and despite leakage on the input node. For example, when RX is high (low) P3 is on and P2 is off (N3 is on and N2 is off), so the leakage of the pull-up (pull-down) branch is due to the low-V_T device P2 (N2); in the same condition, N3 is off and N2 is on (P3 is off and P2 is on), so the leakage of the pull-down (pull-up) network is due to the high-V_T device and is smaller than the leakage related to the complementary branch. This mechanism prevents an undesired fall or rise of RX voltage when the electrode is in the high impedance state. The receiver electrode is smaller than the transmitter electrode; this results in enhanced inter-die coupling and lower sensitivity to alignment while limiting the size of the RX electrode and its parasitic coupling to ground. This interconnection is suitable for a bi-directional realization as well (Fig. 20.1.3). The transmission buffer is replaced by a tri-state one that does not drive the electrode in reception-mode. The receiver subcircuit drives the electrode only during voltage recovery, so it does not require any modification. The initialization circuit for RX is switched-off in transmission-mode, preventing additional power consumption.

The circuits were included in a 0.13μm CMOS test chip (Fig. 20.1.7) conceived for the realization of 3D prototypes by stacking identical chips. Fig. 20.1.4 shows the integrated test structures as well as the waveforms measured, while the communication results are presented in Fig. 20.1.5. For the mono-directional implementation, the transmission of clock signals up to 1.7GHz was verified with electrodes down to 6×6μm^2 (TX electrode is 8×8μm^2) and correct functionality after more than 10^{13} cycles; larger electrodes enable clock transmission up to 2.46GHz. The speed and power depend on the trade-off between parasitic coupling to ground and inter-die coupling: the fastest implementation uses 15×15μm^2 RX electrodes and leads to a 380ps propagation delay with a power consumption of 0.15μW/MHz plus 1.6μW static. Bi-directional circuits show a slightly reduced performance because of the increased circuit complexity; the peak frequency for clock transmission is 1.8GHz with a 20×20μm^2 electrode area. A propagation delay of 560ps was estimated for these structures by a test on more than 10^{12} pseudo-random bits with no error reported (BER < 10^{-12}) and the power consumption is 0.22μW/MHz plus 6μW static.

Fig. 20.1.6 shows a comparison with other 3D solutions and reviews the advancements achieved in both bandwidth and power. The propagation delay reported, together with the capability of transmitting a clock at 1.7GHz through 8×8μm^2 electrodes, provides a throughput per area (max-rate/electrode-area) of more than 22Mb/s/μm^2 with an energy consumption of 80μW/Gb/s. Fig. 20.1.6 highlights the performance trends of capacitive and inductive 3D interconnections. The inductive approach is current-driven and enables an effective face-up assembly but requires large power consumption (1.7mW/Gb/s [4]). The capacitive solution is voltage-driven and this results in lower power consumption, while face-to-face assembly and fine alignment lead to smaller interconnections and this advances the throughput per area. Fig. 20.1.6 also compares this work with through-silicon-vias (TSV) and System-in-Package (SiP) approaches. The reported TSV are 2.5μm per side but require a distance to gate oxide (and thus to functional circuits) of 11μm [8]. The AC electrodes have an area of 8×8μm^2, but they do not affect the silicon substrate so that adjacent circuits can be as close as is allowed by the CMOS design rules; for this reason the pitch enabled by the approach here is, in our judgment, equivalent to TSV. SiP solutions allow die connection using well known technologies, such as microbumps, but suffer from a large interconnection pitch (50-60μm [9, 10]) and from a limited throughput (123Mb/s/pin [9]).

Acknowledgments:
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References:
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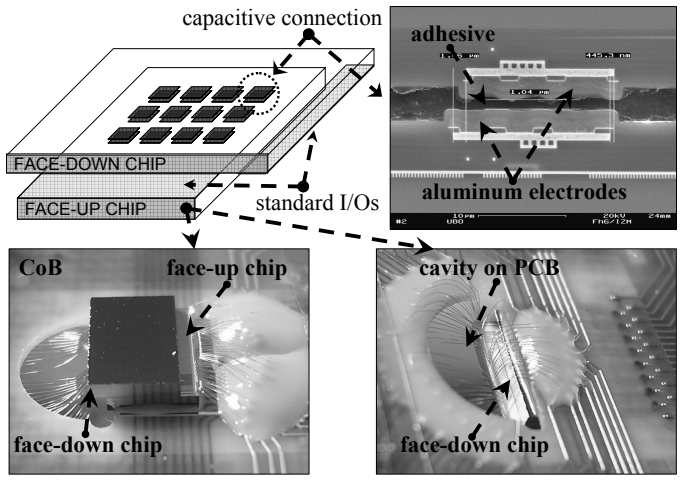


Figure 20.1.1: 3D Capacitive Technology.

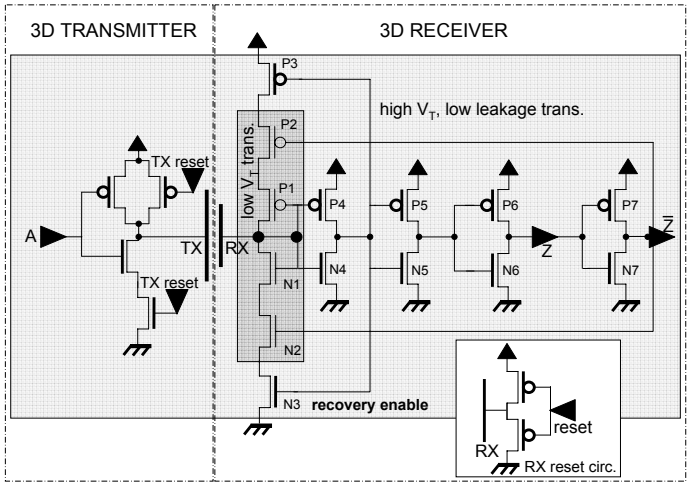


Figure 20.1.2: Mono-directional AC connections.

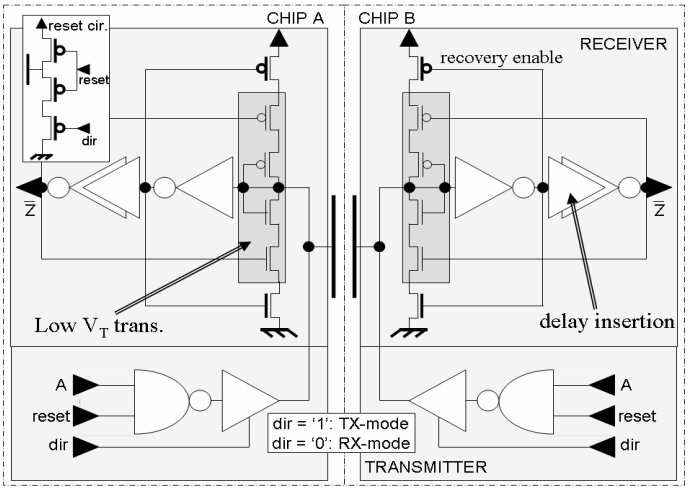


Figure 20.1.3: Bi-directional AC connections.

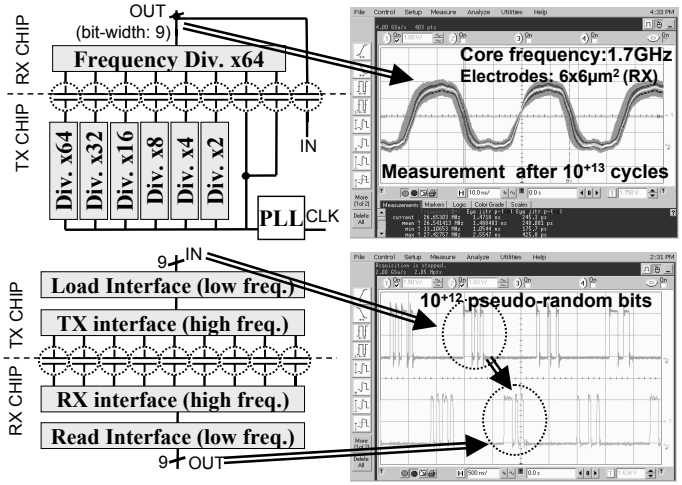
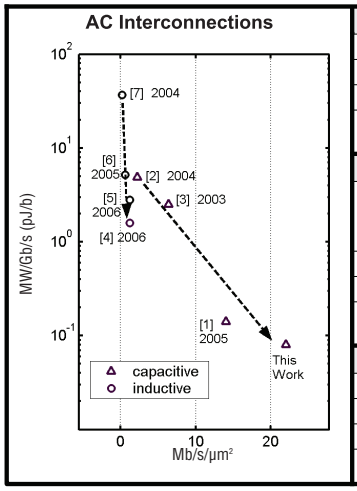


Figure 20.1.4: Test structures and measurement waveforms.

Mono-Directional			Bi-Directional		
Side	**Delay**	**Clock TX**	**Side**	**Delay**	**Clock TX**
RX: 6μm TX: 8μm	420ps	1.7GHz	**15μm**	615ps	1.5GHz
RX: 8μm TX: 10μm	395ps	2.3GHz	**20μm**	560ps	1.8GHz
RX: 10μm TX: 15μm	385ps	2.35GHz	**25μm**	610ps	1.65GHz
RX: 15μm TX: 20μm	380ps	2.46GHz	**29μm**	640ps	1.32GHz
POWER	0.15μW/MHz + 1.6μW Equivalent to 80μW/Gb/s		**POWER**	0.22μW/MHz + 6μW Equivalent to 120μW/Gb/s	
Design Summary	0.13μm CMOS,1.2V. 216 Mono- and Bi-directional links in 3x3 Arrays PLL for clock generation Test-structures for random pattern tests Test-structures for clock transmission tests				**210mW @ 1.2GHz**

Figure 20.1.5: Experimental Results.



This Work	
size	8x8μm²
load	6fF
speed	420ps propagation delay
tech.	Alignment, stacking, external connections
Through Silicon Vias [8]	
size	2.5x2.5μm², 4μm to source/drain, 11μm to gate oxide
load	2.5Ω
speed	N.A.
tech.	Via formation, thinning, soldering, stacking
System In Package [9]	
size	30μm diameter, 60μm pitch
load	50fF, 14mΩ
speed	123Mb/s/pin
tech.	Microbumps, stacking, gluing

Figure 20.1.6: Comparison among 3D technologies.

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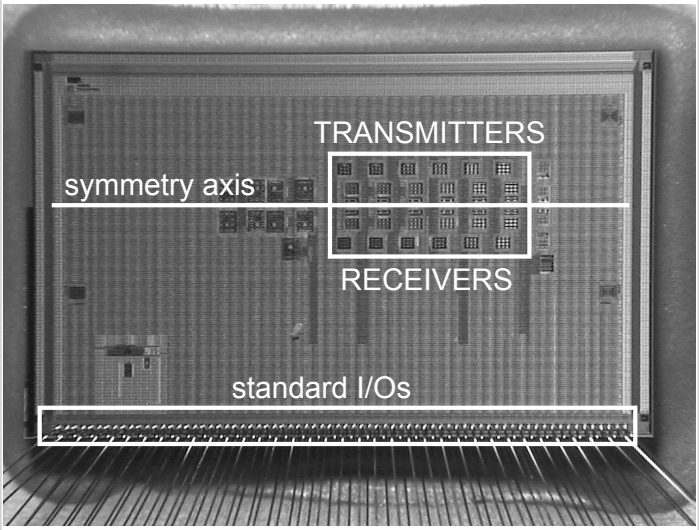

Figure 20.1.7: Micrograph of 6x3.8mm² test-chip, 0.13µm 1.2V CMOS technology.

